80150/80150-2

ADVANCE INFORMATION

iAPX 86/50, 88/50, 186/50, 188/50

CP/M-86 OPERATING SYSTEM PROCESSORS

- **High-Performance Two-Chip Data Processors Containing the Complete CP/M-86 Operating System**
- **Standard On-Chip BIOS (Basic Input/Output System) Contains Drivers for 8272A, 8274, 8255A, 8251A, 7220 Bubble Memory Controller**
- **BIOS Extensible with User-Supplied Peripheral Drivers**
- **User Intervention Points Allow Addition of New System Commands**
- **Memory Disk Makes Possible Diskless CP/M-86 Systems**
- **No License or Serialization Required**
- **Built-in Operating System Timers and Interrupt Controller**
- **8086/80150/80150-2/8088/80186/80188 Compatible At Up To 8 MHz Without Wait States**

The Intel iAPX 86/50, 88/50, 186/50, and 188/50 are two-chip microprocessors offering general-purpose CPU instructions combined with the CP/M-86 operating system. Respectively, they consist of the 8- and 16-bit software compatible 8086, 8088, 80186, and 80188 CPU plus the 80150 CP/M-86 operating system extension.

CP/M-86 is a single-user operating system designed for computers based on the Intel iAPX 86, 88, 186, and 188 microprocessors. The system allows full utilization of the one megabyte of memory available for application programs. The 80150 stores CP/M-86 in its 16K bytes of on-chip memory. The 80150 will run third-party applications software written to run under standard Digital Research CP/M-86.

The 80150 is implemented in N-Channel, depletion-load, silicon-gate technology (HMOS), and is housed in a 40-pin package. Included on the 80150 are the CP/M-86 operating system, Version 1.1, plus hardware support for eight interrupts, a system timer, a delay timer, and a baud rate generator.

*CP/M-86 is a trademark of Digital Research, Inc.

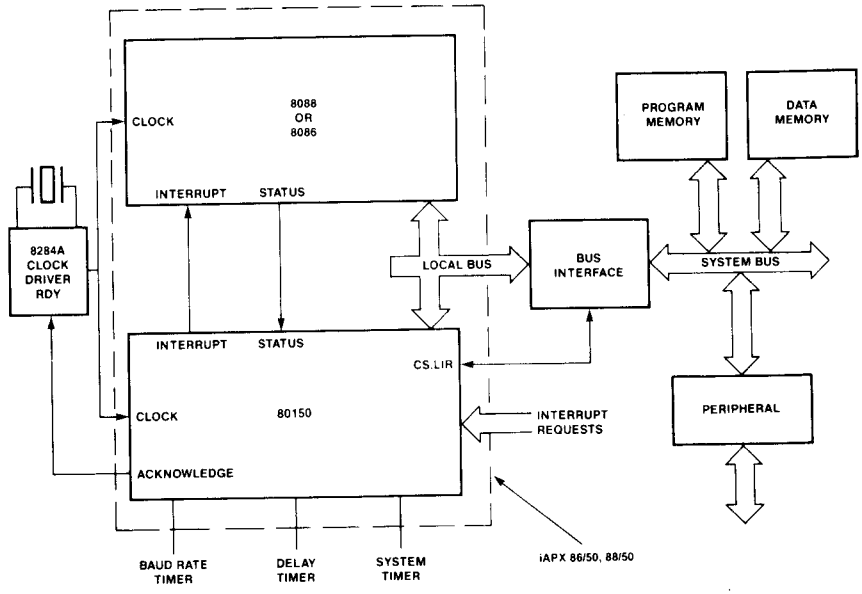


Figure 1. iAPX 86/50, 88/50 Block Diagram

SEPTEMBER 1982
ORDER NUMBER: 210705-002

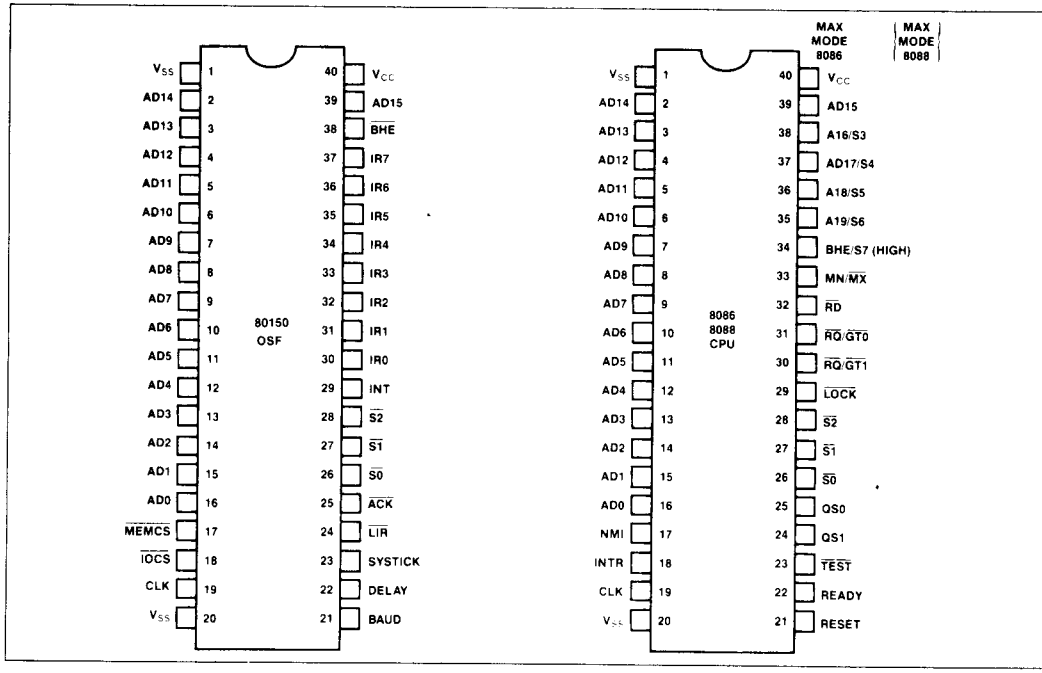


Figure 2. iAPX 86/50, 88/50 Pin Configuration

Table 1. 80150 Pin Description

Symbol	Type	Name and Function
AD_{15}-AD_0	I/O	**Address Data:** These pins constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. These lines are active HIGH. The address presented during T_1 of a bus cycle will be latched internally and interpreted as an 80150 internal address if MEMCS or IOCS is active for the invoked primitives. The 80150 pins float whenever it is not chip selected, and drive these pins only during $T_2 - T_4$ of a read cycle and T_1 of an INTA cycle.
$\overline{BHE}/S_7$	I	**Bus High Enable:** The 80150 uses the BHE signal from the processor to determine whether to respond with data on the upper or lower data pins, or both. The signal is active LOW. BHE is latched by the 80150 on the trailing edge of ALE. It controls the 80150 output data as shown. $\overline{BHE}$ A_0 0 0 Word on AD_{15}-AD_0 0 1 Upper byte on $AD_{15} - AD_8$ 1 0 Lower byte on AD_7-AD_0 1 1 Upper byte on AD_7-AD_0
$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$	I	**Status:** For the 80150, the status pins are used as inputs only. 80150 encoding follows: $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ 0 0 0 INTA 0 0 1 IORD 0 1 0 IOWR 0 1 1 Passive 1 0 0 Instruction fetch 1 0 1 MEMRD 1 1 X Passive

Table 1. 80150 Pin Description (Continued)

Symbol	Type	Name and Function
CLK	I	**Clock:** The system clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The 80150 uses the system clock as an input to the SYSTICK and BAUD timers and to synchronize operation with the host CPU.
INT	O	**Interrupt:** INT is HIGH whenever a valid interrupt request is asserted. It is normally used to interrupt the CPU by connecting it to INTR.
IR_7-IR_0	I	**Interrupt Requests:** An interrupt request can be generated by raising an IR input (LOW to HIGH) and holding it HIGH until it is acknowledged (Edge-Triggered Mode), or just by a HIGH level on an IR input (Level-Triggered Mode).
$\overline{ACK}$	O	**Acknowledge:** This line is LOW whenever an 80150 resource is being accessed. It is also LOW during the first INTA cycle and second INTA cycle if the 80150 is supplying the interrupt vector information. This signal can be used as a bus ready acknowledgement and/or bus transceiver control.
$\overline{MEMCS}$	I	**Memory Chip Select:** This input must be driven LOW when a kernel primitive is being fetched by the CPU. AD_{13}-AD_0 are used to select the instruction.
$\overline{IOCS}$	I	**Input/Output Chip Select:** When this input is low, during an IORD or IOWR cycle, the 80150's kernel primitives are accessing the appropriate peripheral function as specified by the following table: $\overline{BHE}$ A_3 A_2 A_1 A_0 0 X X X X Passive X X X X 1 Passive X 0 1 X X Passive 1 0 0 X 0 Interrupt Controller 1 1 0 0 0 Systick Timer 1 1 0 1 0 Delay Counter 1 1 1 0 0 Baud Rate Timer 1 1 1 1 0 Timer Control
$\overline{LIR}$	O	**Local Bus Interrupt Request:** This signal is LOW when the interrupt request is for a non-slave input or slave input programmed as being a local slave.
V_{CC}		**Power:** V_{CC} is the +5V supply pin.
V_{SS}		**Ground:** V_{SS} is the ground pin.
SYSTICK	O	**System Clock Tick:** Timer 0 Output.
DELAY	O	**DELAY Timer:** Output of timer 1.
BAUD	O	**Baud Rate Generator:** 8254 Mode 3 compatible output. Output of 80150 Timer 2.

The 80150 breaks new ground in operating system software-on-silicon components. It is unique because it is the first time that an industry-standard personal/small business computer operating system is being put in silicon. The 80150 contains Digital Research's CP/M-86 operating system, which is designed for Intel's line of software- and interface-compatible iAPX 86, 88, 186, and 188 microprocessors. Since the entire CP/M-86 operating system is contained on the chip, it is now possible to design a diskless computer that runs proven and commonly available applications software. The 80150 is a true operating system extension to the host microprocessor, since it also integrates key operating system-related peripheral functions onto the chip.

MODULAR DESIGN

Based on a proven, modular design, the system includes the:

- CCP: Console Command Processor

  The CCP is the human interface to the operating system and performs decoding and

execution of user commands.

- BDOS: Basic Disk Operating System

  The BDOS is the logical, invariant portion of the operating system; it supports a named file system with a maximum of 16 logical drives, containing up to 8 megabytes each for a potential of 128 megabytes of on-line storage.

- BIOS: Basic Input/Output System

  The physical, variant portion of the operating system, the BIOS contains the system-dependent input/output device handlers.

CP/M* COMPATIBILITY

CP/M-86 files are completely compatible with CP/M for 8080- and 8085-based microcomputer systems. This simplifies the conversion of software developed under CP/M to take full advantage of iAPX 86, 88, 186, 188-based systems.

The user will notice no significant difference between CP/M and CP/M-86. Commands such as DIR, TYPE, REN, and ERA respond the same way in both systems.

CP/M-86 uses the iAPX 86, 88, 186, 188 registers corresponding to 8080 registers for system call and return parameters to further simplify software transport. The 80150 allows application code and data segments to overlap, making the mixture of code and data that often appears in CP/M applications acceptable to the iAPX 86, 88, 186, 188.

Unique Capabilities of CP/M-86 in Silicon

1. CP/M-86 on-a-chip reduces software development required by the system designer. It can change the implementation of the operating system into the simple inclusion of the 80150 on the CPU board.

   As described later, the designer can either simply incorporate the Intel chip without the need for writing even a single line of additional code, or he can add additional device drivers by writing only the small amount of additional code required.

2. The 80150 is the most cost-effective way to implement CP/M-86 in a microcomputer. The integration of CP/M-86 with the 16K bytes of system memory it requires, the two boot ROMS required in a diskette-based CP/M-86, and the on-chip peripherals (interrupt controller and timers) lead to savings in software, parts cost, board space, and interconnect wiring.

3. The reliability of the microcomputer is increased significantly. Since CP/M-86 is now always in the system as a standard hardware operating system, a properly functioning system diskette is not required. CP/M-86 in hardware can no longer be overwritten accidentally by a runaway program. System reliability is enhanced by the decreased dependence on floppy disks and fewer chips and interconnections required by the highly integrated 80150.

4. The microcomputer system boots up CP/M-86 on power-on, rather than requiring the user to go through a complicated boot sequence, thus lowering the user expertise required.

5. Diskless CP/M-based systems are now easy to design. Since CP/M is already in the microcomputer hardware, there is no need for a disk drive in the system if it is not desired. Without a disk drive, a system is more portable, simpler to use, less costly, and more reliable.

6. The administrative costs associated with distributing CP/M-86 are eliminated. Since CP/M-86 is now resident on the 80150 in the microcomputer system, there is no end-user licensing required nor is there any serialization requirement for the 80150 (because no CP/M diskette is used).

7. End-users will value having their CP/M operating system resident in their computer rather than on a diskette. They will no longer have to back up the operating system or have a diskette working properly to bring the system up in CP/M, increasing their confidence in the integrity, reliability, and usability of the system.

80150 FUNCTIONAL DESCRIPTION

The 80150 is a processor extension that is fully compatible with the 8086, 8088, 80186, and 80188 microprocessors. When the 80150 is combined with the microprocessor, the two-chip set is called an Operating System Processor and is denoted as the iAPX 86/50, 88/50, 186/50, or 188/50. The basic system configuration is shown in Figure 1. The 80150 connects directly to the multiplexed address/data bus and runs up to 8 MHz without wait states.

A. Hardware. Figure 3 is a functional diagram of the 80150 itself. CP/M-86 is stored in the 16K-bytes of control store. The timers are compatible with the standard 8254 timer. The interrupt controller, with its eight programmable interrupt inputs and one interrupt output, is compatible with the 8259A Programmable Interrupt Controller. External slave 8259A inter-

*CP/M is a registered trademark of Digital Research, Inc.

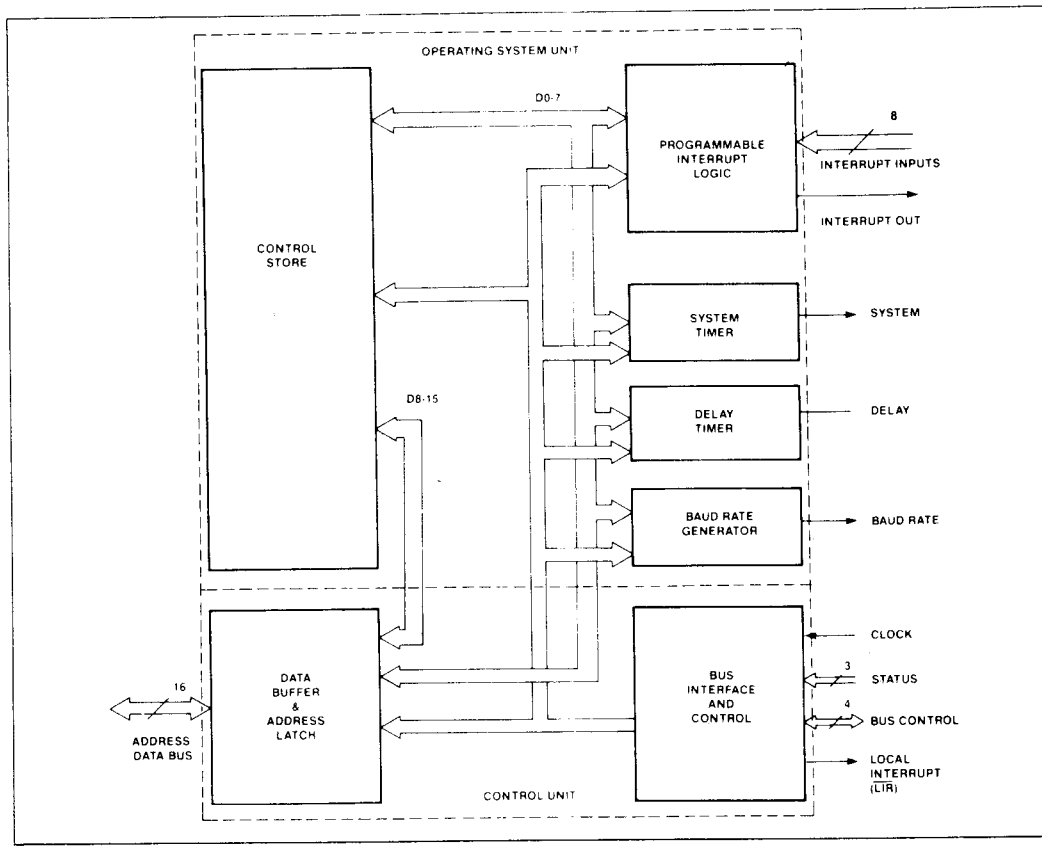


Figure 3. 80150 Internal Block Diagram

rupt controllers can be cascaded with the 80150 to expand the total number of interrupts to 57.

B. Software. Digital Research's version 1.1 of CP/M-86 forms the basis of the 80150. CP/M consists of three major parts: the Console Command Processor (CCP), the Basic Disk Operating System (BDOS), and the Basic Input/Output System (BIOS). Details on CP/M-86 are provided in Digital Research's *CP/M-86 Operating System User's Guide* and *CP/M-86 Operating System System Guide.*

CCP - Console Command Processor

The CCP provides all of the capabilities provided by Digital Research's CCP. Built-in commands have been expanded to include capabilities normally included as transient utilities on the Digital Research CP/M-86 diskette. Commands are provided to format diskettes, transfer files between devices (based on Digital Research's Peripheral Interchange Program PIP), and alter and display I/O device and file status (based on Digital Research's STAT).

Through User Intervention Points, the standard CP/M-86 CCP is enhanced to allow the user to add new built-in commands to further customize a CP/M-86 system.

BDOS - Basic Disk Operating System

Once the CCP has parsed a command, it sends it to the BDOS, which performs system services such as managing disk directories and files. Some of the standard BDOS functions provide:

Console Status
Console Input and Output
List Output
Select Drive
Set Track and Sector

Read/Write Sector
Load Program

The BDOS in the 80150 provides the same functions as the standard Digital Research CP/M-86 BDOS.

BIOS - Basic Input/Output System

The BIOS contains the system-dependent I/O drivers. The 80150 BIOS offers two fundamental configuration options:

1. **A predefined configuration** which supports minimum cost CP/M-86 microcomputer systems and which requires no operating system development by the system designer.
2. **An OEM-configurable mode,** where the designer can choose among several drivers offered on the 80150 or substitute or add any additional device drivers of his choice.

These two options negate the potential software-on-silicon pitfall of inflexibility in system design. The OEM can customize the end system as desired.

The **predefined configuration** offers a choice among several peripheral chip drivers included on the 80150. Drivers for the following chips are included in the 80150 BIOS:

8251A	Universal Synchronous/ Asynchronous Receiver/Transmitter (USART)
8274	Multi-Protocol Serial Controller (MPSC)
8255A	Programmable Parallel Interface (PPI)
8272A	Floppy Disk Controller
7220	Bubble Memory Controller

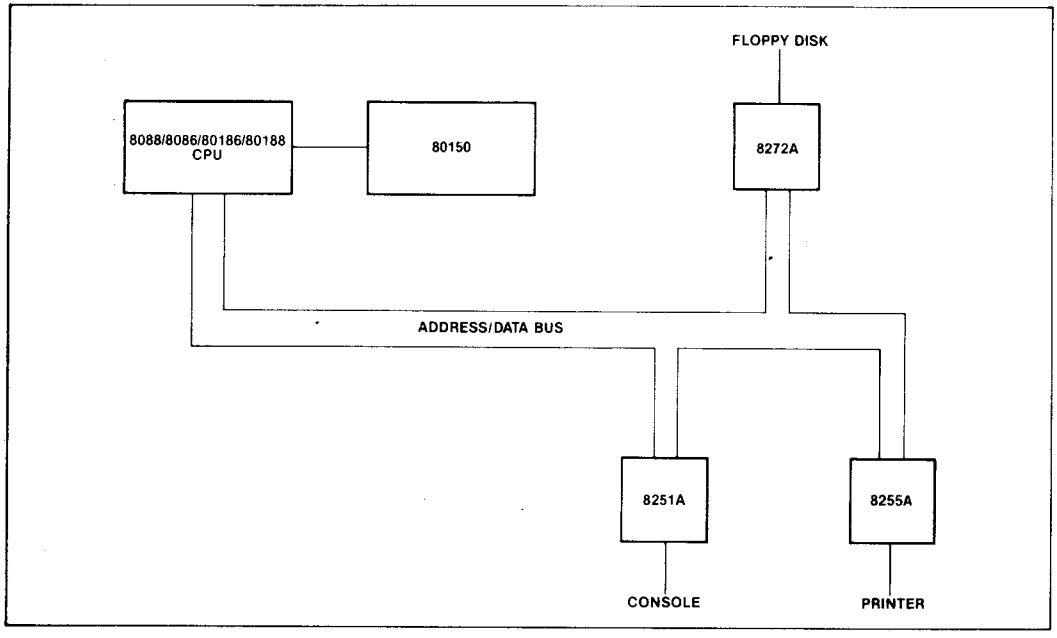


Figure 4. Predefined Configuration

Even in the predefined configuration, the system designer (or end user, if the system designer desires) may select parameters such as the baud rates for the console and printer, and the floppy disk size (standard 8″ or 5¼″ mini-floppy) and format (FM single density or MFM double density, single-sided or double-sided).

Drivers for the 80150 on-chip timers and interrupt controller are also included in the BIOS.

The 80150 takes advantage of the 80186 and 80188 on-chip peripherals in an iAPX 186/50 or 188/50 system. For example, the integrated DMA controller is used. Also fully utilized are the integrated memory chip selects and I/O chip selects.

Since all microcomputer configurations cannot be anticipated, the **OEM-configurable mode** allows the system designer to use any set of peripheral chips desired. This configuration is shown in Figure 5.

By simply changing the jump addresses in a configuration table, the designer can also gain the flexibility of adding custom BIOS drivers for other peripheral chips, such as bubble memories or more complex CRT controllers. These drivers would be stored in memory external to the 80150 itself. By providing the configurability option, the 80150 is applicable to a far broader range of designs that it would be with an inflexible BIOS.

MEMORY ORGANIZATION

When using the **predefined configuration** of the 80150 BIOS, the 80150 must be placed in the top 16K of the address space of the microprocessor (starting at location FC000H) so that the 80150 gains control when the microprocessor is reset. Upon receipt of control, the 80150 writes a **configuration block** into the bottom of the microprocessor's address space, which must be in RAM. The 80150 uses the area after the interrupt vectors for system configuration information and scratch-pad storage.

When using the **OEM-configurable** mode of the 80150 BIOS, the 80150 is placed on any 16K boun-

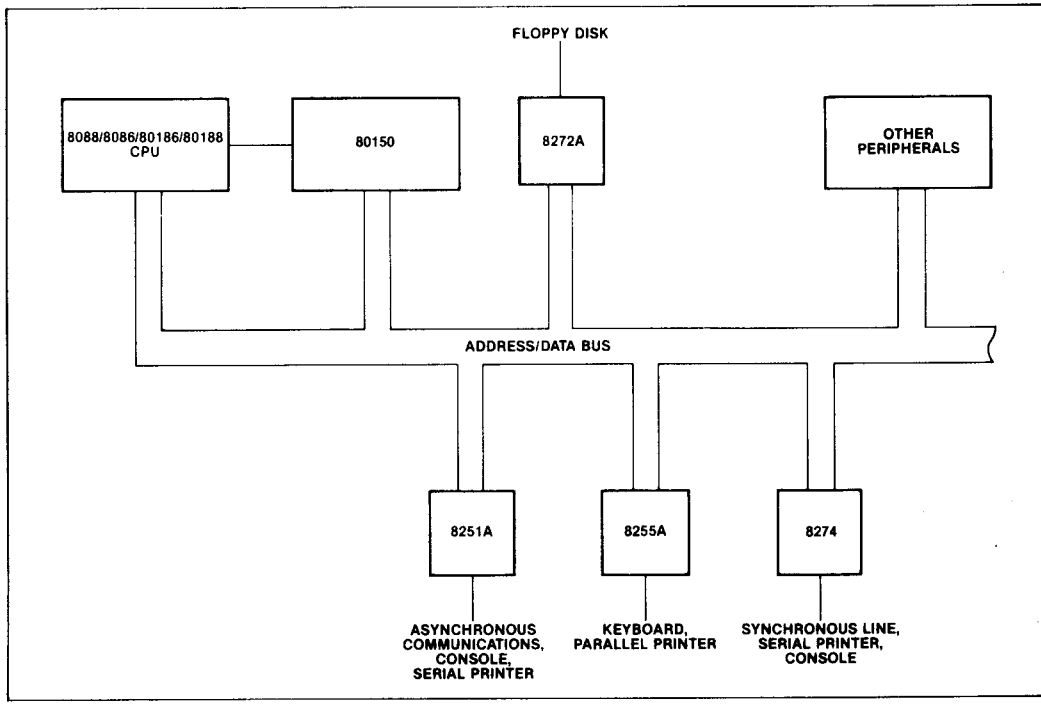


Figure 5. OEM Configurable System

dary of memory **except** the highest (FC000H) or lowest (00000H). The user writes interface code (in the form of a simple boot ROM) to incorporate and link additional features and changes into the standard 80150 environment. The configuration block may be located as desired in the address space, and its size may vary widely depending on the application.

Memory Disk and Bubble Memories

A unique capability offered by the 80150 is the Memory Disk. The Memory Disk consists of a block of RAM whose size can be selected by the designer. The Memory Disk is treated by the BDOS as any standard floppy disk, and is one of the 16 disks that CP/M can address. Thus files can be opened and closed, programs stored, and statistics gathered on the amount of Memory Disk space left.

The 80150 also contains software drivers for 7220 bubble memory controller. Use of a bubble memory board as a substitute for one floppy disk drive is directly supported.

The Memory Disk opens the possibility of a portable low-cost diskless microcomputer or network station. Applications software can be provided in a number of ways:

a. telephone lines via a modem.
b. ROM-based software.
c. a network.
d. bubble memory based software.
e. low-cost cassettes.

TYPICAL SYSTEM CONFIGURATION

Figure 6 shows the processing cluster of a "typical" iAPX 86/50 or iAPX 88/50 OSP system. Not shown are subsystems likely to vary with the application. The configuration includes an 8086 (or 8088) operating in maximum mode, an 8284A clock generator and an 8288 system controller. Note that the 80150 is located on the CPU side of any latches or transceivers.

Timers

The Timers are connected to the lower half of the data bus and are addressed at even addresses. The timers are read as two successive bytes,

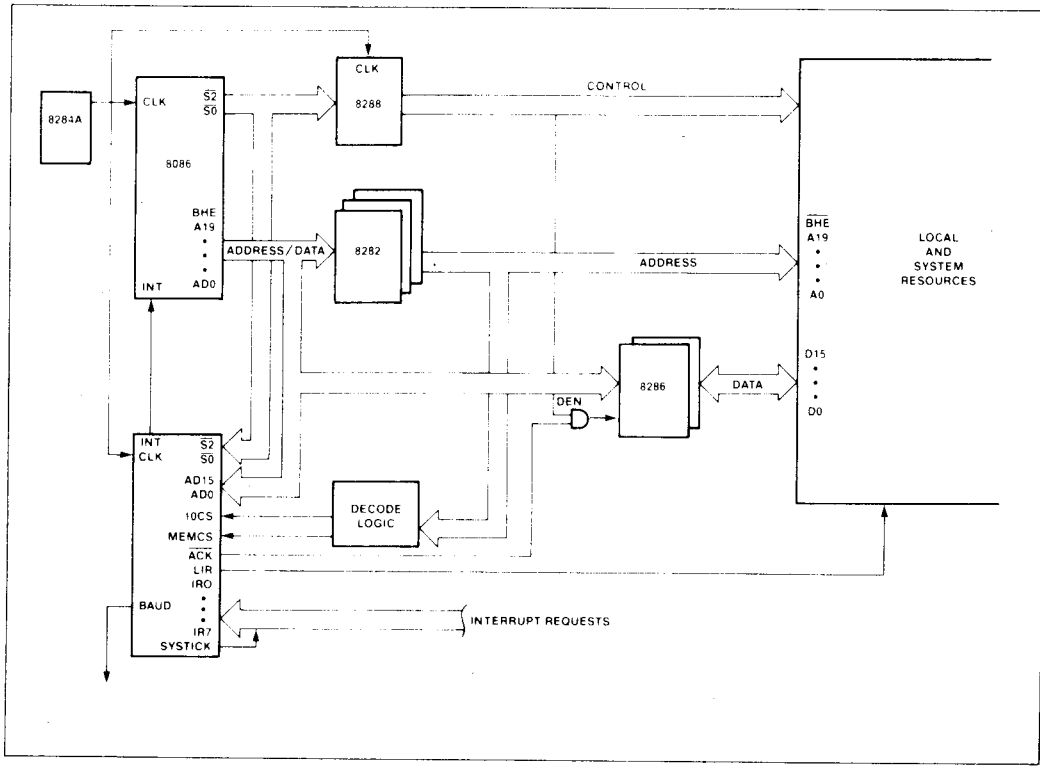


Figure 6. Typical OSP Configuration

always LSB followed by MSB. The MSB is always latched on a read operation and remains latched until read. Timers are not gatable. An external 8254 Programmable Interval Timer may be added to the system.

Baud Rate Generator

The baud rate generator operates like an 8254 (square wave mode 3). Its output, BAUD, is initially high and remains high until the Count Register is loaded. The first falling edge of the clock after the Count Register is loaded causes the transfer of the internal counter to the Count Register. The output stays high for N/2 [(N + 1)/2 if N is odd] and then goes low for N/2 [(N – 1)/2 if N is odd]. On the falling edge of the clock which signifies the final count for the output in low state, the output returns to high state and the Count Register is transferred to the internal counter. The baud rates can vary from 300 to 9600 baud.

The baud rate generator is located at 0CH (12), relative to the 16-byte boundary in the I/O space in which the 80150 component is located. The timer control word is located at relative address, 0EH(14). Timers are addressed with IOCS = 0. Timers 0 and 1 are assigned to use by the OSP, and should not be altered by the user.

The 80150 timers are subset compatible with 8254 timers.

Interrupt Controller

The Programmable Interrupt Controller (PIC), is also an integral unit of the 80150. Its eight input pins handle eight vectored priority interrupts. One of these pins must be used for the SYSTICK time function in timing waits, using an external connection as shown. During the 80150 initialization and configuration sequence, each 80150 interrupt pin is individually programmed as either level or edge sensitive. External slave 8259A interrupt controllers can be used to expand the total number of interrupts to 57.

In addition to standard PIC functions, the 80150 PIC unit has an $\overline{LIR}$ output signal, which when low indicates an interrupt acknowledge cycle. $\overline{LIR} = 0$ is provided to control the 8289 Bus Arbiter SYSB/RESB pin. This will avoid the need of requesting the system bus to acknowledge local bus non-slave interrupts. The user defines the interrupt system as part of the configuration.

INTERRUPT SEQUENCE

The interrupt sequence is as follows:

1. One or more of the interrupts is set by a low-to-high transition on edge-sensitive IR inputs or by a high input on level-sensitive IR inputs.
2. The 80150 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an interrupt acknowledge cycle which is encoded in $\overline{S_2} - \overline{S_0}$.
4. Upon receiving the first interrupt acknowledge from the CPU, the highest-priority interrupt is set by the 80150 and the corresponding edge detect latch is reset. The 80150 does not drive the address/data bus during this bus cycle but does acknowledge the cycle by making $\overline{ACK} = 0$ and sending the $\overline{LIR}$ value for the IR input being acknowledged.
5. The CPU will then initiate a second interrupt acknowledge cycle. During this cycle, the 80150 will supply the cascade address of the interrupting input at T_1 on the bus and also release an 8-bit pointer onto the bus if appropriate, where it is read by the CPU. If the 80150 does supply the pointer, then $\overline{ACK}$ will be low for the cycle. This cycle also has the value $\overline{LIR}$ for the IR input being acknowledged.
6. This completes the interrupt cycle. The ISR bit remains set until an appropriate EXIT INTERRUPT primitive (EOI command) is called at the end of the Interrupt Handler.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin With
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 1.0 Watts

NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + .5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
I_{CC}	Power Supply Current		200	mA	T_A = 25 C
I_{LI}	Input Leakage Current		10	μA	$0 < V_{IN} < V_{CC}$
I_{LR}	IR Input Load Current		10 −300	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0$
I_{LO}	Output Leakage Current		10	μA	$.45 \le V_{IN} \le V_{CC}$
V_{CLI}	Clock Input Low		0.6	V	
V_{CHI}	Clock Input High	3.9		V	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		15	pF	
I_{CLI}	Clock Input Leakage Current		10 150 10	μA μA μA	$V_{IN} = V_{CC}$ V_{IN} = 2.5V V_{IN} = 0V

A.C. CHARACTERISTICS (T_A = 0-70°C, V_{CC} = 4.5-5.5 Volt, V_{SS} = Ground)

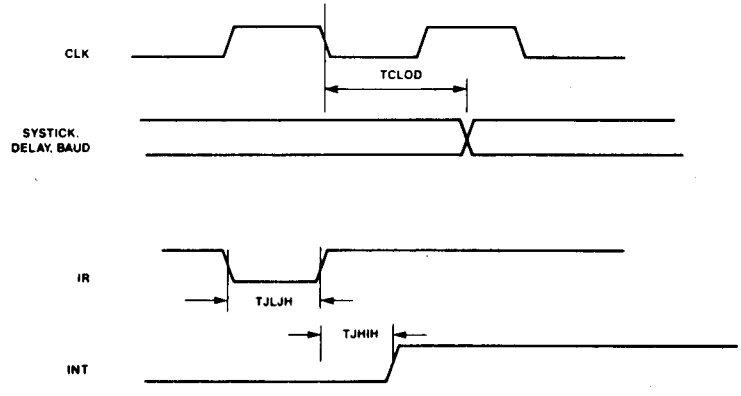
		80150		80150-2			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Test Conditions
T_{CLCL}	CLK Cycle Period	200	–	125	–	ns	
T_{CLCH}	CLK Low Time	90	–	55	–	ns	
T_{CHCL}	CLK High Time	69	2000	44	2000	ns	
T_{SVCH}	Status Active Setup Time	80	–	65	–	ns	
T_{CHSV}	Status Inactive Hold Time	10	–	10	–	ns	
T_{SHCL}	Status Inactive Setup Time	55	–	55	–	ns	
T_{CLSH}	Status Active Hold Time	10	–	10	–	ns	
T_{ASCH}	Address Valid Setup Time	8	–	8	–	ns	
T_{CLAH}	Address Hold Time	10	–	10	–	ns	
T_{CSCL}	Chip Select Setup Time	20	–	20	–	ns	
T_{CHCS}	Chip Select Hold Time	0	–	0	–	ns	
T_{DSCL}	Write Data Setup Time	80	–	60	–	ns	
T_{CHDH}	Write Data Hold Time	10	–	10	–	ns	
T_{JLJH}	IR Low Time	100	–	100	–	ns	
T_{CLDV}	Read Data Valid Delay	–	140	–	105	ns	C_L = 200 pF
T_{CLDH}	Read Data Hold Time	10	–	10	–	ns	
T_{CLDX}	Read Data to Floating	10	100	10	100	ns	
T_{CLCA}	Cascade Address Delay Time	–	85	–	65	ns	

A.C. CHARACTERISTIC (Continued)

		80150		80150-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Notes**
T_{CLCF}	Cascade Addresse Hold Time	10	–	10	–	ns	
T_{IAVE}	INTA Status t Acknowledge	–	80	–	80	ns	
T_{CHEH}	Acknowledge Hold Time	0	–	0	–	ns	
T_{CSAK}	Chip Select to ACK	–	110	–	110	ns	
T_{SACK}	Status to ACK	–	140	–	140	ns	
T_{AACK}	Address to ACK	–	90	–	90	ns	
T_{CLOD}	Timer Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{CLOD1}	Timer1 Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{JHIH}	INT Output Delay	–	200	–	200	ns	
T_{IRCL}	IR Input Set Up	20		20		ns	

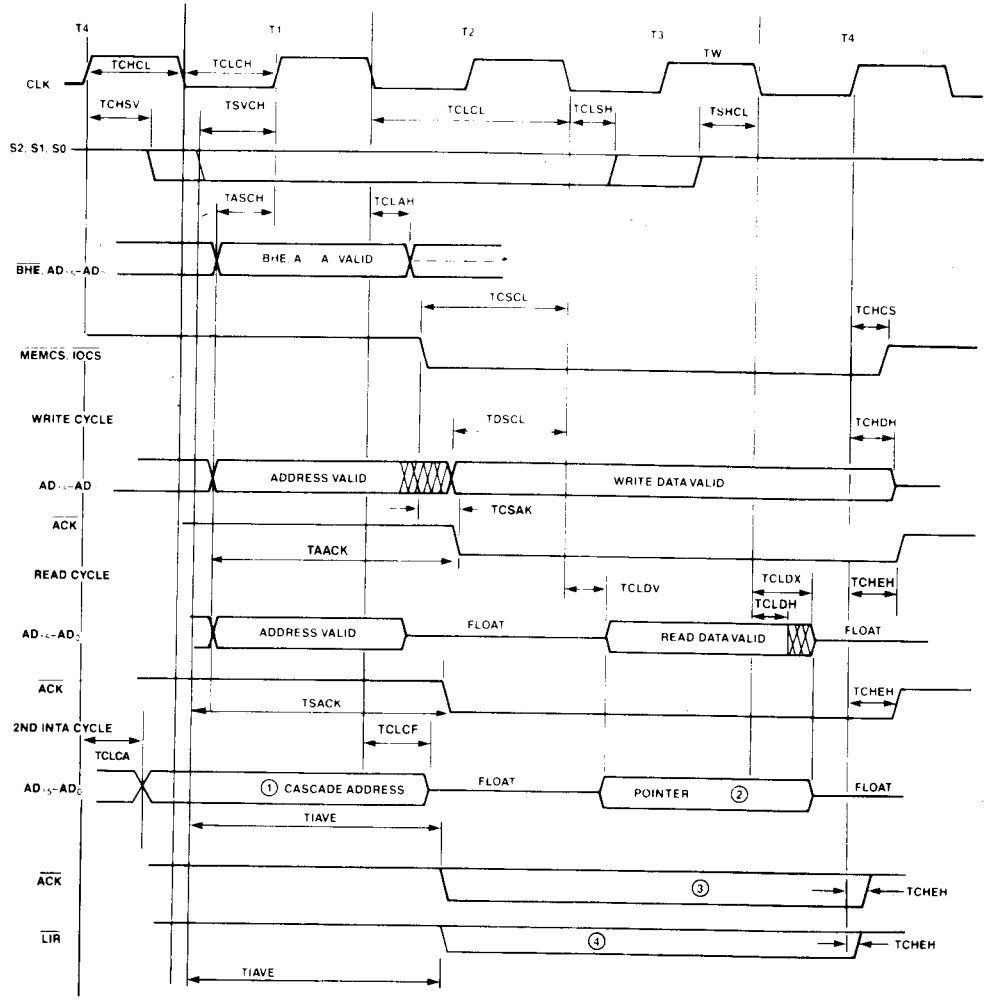
WAVEFORMS

A.C.



WAVEFORMS

A.C.



NOTES
1. CASCADE ADDRESS PRESENTED ON AD8, AD9 AND AD10 CORRESPONDING TO CAS0, CAS1 AND CAS2 RESPECTIVELY. AD11-AD15 LINES ARE ACTIVE AND HAVE UNKNOWN VALUES. AD0-AD7 ARE TRISTATE.
2. POINTER VALUE IS ACTIVE ONLY IF POINTER IS GENERATED FROM THE 80150 AND NOT FROM EXTERNAL SLAVE UNIT.
3. ACTIVE LOW ONLY WHEN POINTER DATA IS BEING SUPPLIED BY THE 80150.
4. LOW ONLY FOR LOCAL INTERRUPT.